S/N 10/023819 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Biju Chandran et al.

Examiner:

John Vigushin

Serial No.:

10/023819

Group Art Unit:

2827

Filed:

December 21, 2001

Docket:

884.A27US1

Title:

CHIP-JOIN PROCESS TO REDUCE ELONGATION MISMATCH BETWEEN

THE ADHERENTS AND SEMICONDUCTOR PACKAGE MADE THEREBY

Assignee:

Intel Corporation

Customer No:

21186

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Applicants note that certain of the enclosed references were first received in a communication from a foreign patent office in a counterpart foreign application. A copy of the relevant International Search Report, in PCT/IS02/36038, is also enclosed.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

INFORMATION DISCLOSURE STATEMENT

Serial No: 10/023819

Filing Date: December 21, 2001

Title: CHIP-JOIN PROCESS TO REDUCE ELONGATION MISMATCH BETWEEN THE ADHERENTS AND SEMICONDUCTOR

PACKAGE MADE THEREBY

Assignee: Intel Corporation

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

BIJU CHANDRAN ET AL.

By their Representatives,

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Dkt: 884.A27US1 (INTEL)

Date March 18, 2004 By Conn

Ann McCrackin Reg. No. 42,858

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being hand-delivered to: US Patent and Trademark Office, 2011 South Clark Place, Customer Window, Mail Stop 313(c), Crystal Plaza Two, Lobby, Room 1B03, Arlington, VA 22202, on this 197H day of March, 2004.

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for the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number. Substitute for form 1449A/PTO Complete if Known INFORMATION DISCLOSURE 10/023819 **Application Number** STATEMENT BY APPLICANT December 21, 2001 Filing Date **First Named Inventor** Chandran, Biju 2827 **Group Art Unit** MAR 1-9 2004 **Examiner Name** Vigushin, John Attorney Docket No: 884.A27US1 Sheet 1 of 1

	US PATENT DOCUMENTS									
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	OTHE	R DOCUMENTS NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
		ANONYMOUS, "Solder ball for semiconductor chip - has height increased so that stress caused by difference in thermal expansion between chip and substrate is minimised", Research Disclosure RD-291011, Derwent 1988-255069, (7/10/88), 2 pages	